Modeling the Substrate Effect in Interconnect Line Characteristics of High-Speed VLSI Circuits

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***Abstract*— A new analytic model for interconnect characteristics is proposed. The model includes the frequency-dependent distribution of the current on the interconnect lines and the substrate as the current path. The validity of the proposed model has been checked by a comparison with the measurement data and the numerical simulation. Through this work, it is found that the substrate return path must be considered for the accurate prediction of the high-frequency characteristics of interconnects.**

I. Introduction

THE determination of electrical properties of interconnects represents a critical design and analysis problem in the high-speed integrated very large-scale integration (VLSI) circuit in order to minimize signal distortion due to propagation delay and dispersion [1]. In order to accomplish this, it is necessary to analyze and model the broad-band characteristics [2]–[5] of the interconnects since the signals tend to exhibit both the short rising and falling times. The transmission behavior of lines on semi-insulating substrates (such as GaAs) has already been extensively investigated, and reasonable models for their electrical properties have been reported. However, for the case of a conductive substrate such as doped silicon, the effect of the doped substrate on the transmission behavior of the interconnects has not been well modeled with an analytical closed formula. The effect of a silicon substrate, which is negligible at low frequency, has a prevalent effect on the characteristics of lines during the operation of high-speed chips [2], [3].

In this paper, we describe an analytical model for interconnect characteristics (including the substrate) as a current return path, and the evaluation of its validity by comparing some numerical simulations and measurements. This paper is organized as follows: an analytical model including a substrate as the return path is derived, followed by a comparison with measurements and numerical simulations. Finally, discussions and a conclusion are followed.

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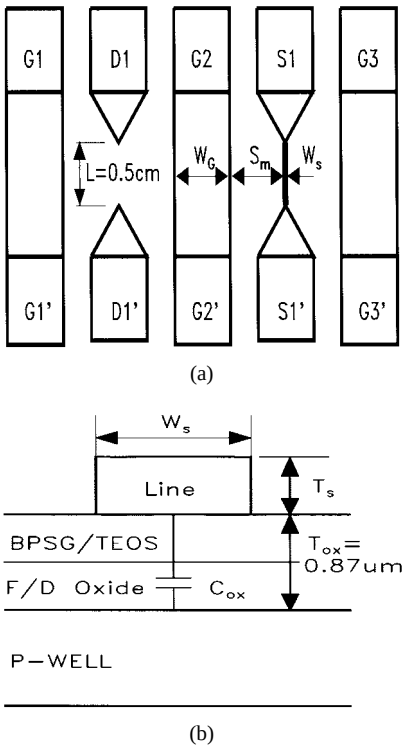
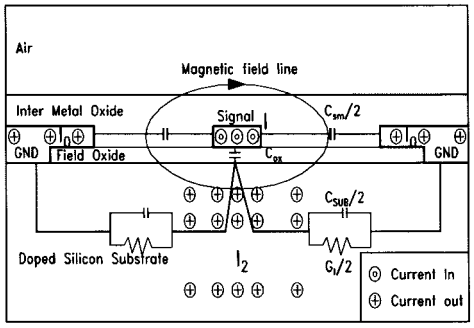


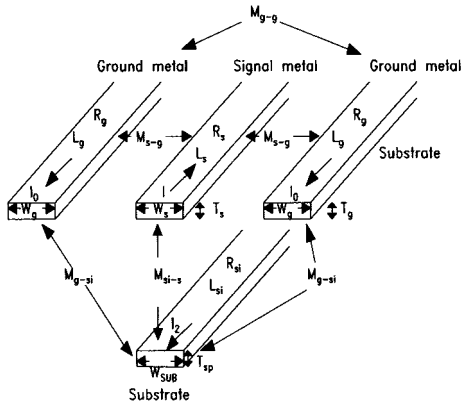
Fig. 1. Single-line test structure for the use of Cascade Microtech ground–signal–ground (GSG) probes. Signal lines are split into W_s = 1-, 2-, 4-, 10-, and 20-μm widths and ground line widths are fixed at 100 μm. Pad-to-pad spacing is fixed at 50 μm. The geometric information is listed in Table I. (a) Top view of the test structure. (b) Cross-sectional view of (a).

II. Analytical Modeling

We consider a new model of a metal–insulator–semiconductor (MIS) coplanar line where two ground lines are connected to the silicon substrate and the signal line is located at the center between these ground lines, as shown in Fig. 1. The width and thickness of the lines are W_g, T_g and W_s, T_s for the ground line and signal line, respectively. The structure can be represented by circuit elements for impedances and admittances of a coplanar line system. The geometrical descriptions and definitions of the impedances of each line in Figs. 1 and 2 are tabulated in Tables I–III. Each line has a resistance of R_i, a self inductance of L_i, and a mutual inductance M_{i-j} (i and $j = g$, s, and SUB) per unit length, as shown in Fig. 2(a). The substrate effect is included by considering mutual inductance with other lines and the current component I_2, as shown in Fig. 2(b). The current through the signal line I can be expressed by the



(a)



(b)

Fig. 2. (a) Cross-sectional view of MIS coplanar lines consisting of ground lines with ohmic contacts on the silicon substrate and its impedance (admittance) system. (b) Schematics of the MIS system.

TABLE I
GEOMETRICAL DESCRIPTION OF THE ELEMENTS SHOWN IN FIGS. 1(a), 1(b) and 2(a)

Symbols	Definition
W_s	signal line width
W_g	ground line width
W_{SUB}	effective substrate width served as current return path
T_s	signal line thickness
T_g	ground line thickness
T_{ox}	oxide thickness layered under lines
T_{sp}	substrate skin depth
S_m	spacing between signal line and ground line

return currents defined as I_0 through a ground line and I_2 through a substrate, respectively, as

$$I = 2I_0 + I_2 = I_1 + I_2 = \alpha I + (1-\alpha)I \qquad (1)$$

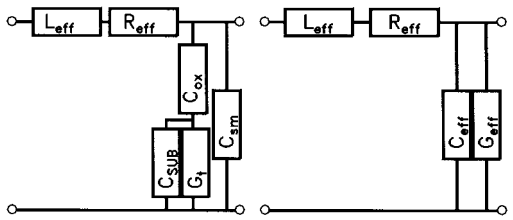
where $\alpha (0 \leq \alpha \leq 1)$ is defined as the ratio of the current through two ground lines over a signal line. Therefore, the system illustrated in Fig. 2 can be schematically transformed to the analytical models, as shown in Fig. 3(a) and (b). Fig. 3(a) can be considered as a pre-equivalent π model whose shunt components have the corresponding component in Fig. 2(a). The final equivalent π model elements ($L_{\rm eff}$, $R_{\rm eff}$, $C_{\rm eff}$, and $G_{\rm eff}$) of the system in Fig. 3(b) can be compared with interconnect characteristics extracted from the scattering-parameter measurements.

TABLE II
DEFINITION OF THE IMPEDANCES USED IN THE PROPOSED MODELING. DETAILED FORMULA ARE GIVEN IN THE APPENDIX

Symbols	Definition
L_s	self inductance of signal line
L_g	self inductance of ground line
L_{SUB}	self inductance of current path on a substrate (self inductance of silicon path)
$M_{s\text{-}g}$	Mutual inductance between signal line to ground line
$M_{s\text{-}SUB}$	Mutual inductance between signal line to substrate path
$M_{g\text{-}g}$	Mutual inductance between ground line to ground line
$M_{g\text{-}SUB}$	Mutual inductance between ground line to substrate path
$L_{s,g}$	total inductance of the coplanar line without the substrate : $(L_g+M_{g\text{-}g})/2+L_s-2M_{s\text{-}g}$
$L_{s,SUB}$	total inductance of the quasi-microstrip line with the substrate return path : $L_{SUB}+L_s-2M_{s\text{-}SUB}$
$L_{g,SUB}$	total inductance of the ground lines with the substrate return path : $(L_g+M_{g\text{-}g})/2+L_{SUB}-2M_{g\text{-}SUB}$
R_s	Signal line resistance
R_g	Ground line resistance
R_{SUB}	Longitudinal resistance of a substrate return path

TABLE III
DEFINITION OF THE ADMITTANCES USED IN THE PROPOSED MODELING. DETAILED FORMULA ARE GIVEN IN THE APPENDIX

Symbols	Definitions
C_{ox}	capacitance between the signal line and silicon substrate through oxide regions
C_{SUB}	capacitance between the signal line and ground lines through the substrate
C_{sm}	capacitance between the signal line and ground lines through air
G_t	conductance between the signal line and ground lines



(a) (b)

Fig. 3. Equivalent model of MIS coplanar systems, as shown in Fig. 2. (a) Pre-equivalent model. (b) Final equivalent π model. $L_{\rm eff}$, $R_{\rm eff}$, $C_{\rm eff}$, and $G_{\rm eff}$ are the equivalent distributed inductance, resistance, capacitance, and conductance, respectively. (a) Pre-equivalent π model. (b) Equivalent π model.

First, we represent $L_{\rm eff}$ and $R_{\rm eff}$ with terms such as the inductances and resistances of each line. Using the law of magnetic energy conservation [6], the total magnetic energy

of the system can be expressed using L_{eff} as follows:

$$\begin{aligned}\frac{1}{2}L_{\text{eff}}I^2 &= L_gI_0^2+\frac{1}{2}L_sI^2+\frac{1}{2}L_{\text{SUB}}I_2^2\\ &\quad+2M_{s-g}I_0I+M_{\text{SUB}-s}I_2I+M_{g-g}I_0^2\\ &\quad+2M_{g-\text{SUB}}I_0I_2\\ &=\frac{1}{2}(\alpha^2\frac{1}{2})L_gI^2+\frac{1}{2}L_sI^2+\frac{1}{2}(1-\alpha)^2L_{\text{SUB}}I^2\\ &\quad-\alpha M_{s-g}I^2-(1-\alpha)M_{SUB-s}I^2\\ &\quad+\frac{1}{2}\left(\alpha^2\frac{1}{2}\right)M_{g-g}I^2+\alpha(1-\alpha)M_{g-SUB}I^2. \quad (2)\end{aligned}$$

After rearranging (2), L_{eff} can be expressed by the total inductances $L_{s,g}$, $L_{s,SUB}$, and $L_{g,SUB}$, defined in Table II, as

$$\begin{aligned}L_{\text{eff}} &=\alpha\left[\frac{1}{2}(L_g+M_{g-g})+L_s-2M_{s-g}\right]\\ &\quad+(1-\alpha)[L_{\text{SUB}}+L_s-2M_{\text{SUB}-s}]\\ &\quad-\alpha(1-\alpha)\left[\frac{1}{2}(L_g+M_{g-g})+L_{\text{SUB}}-2M_{g-\text{SUB}}\right]\\ &=\alpha L_{s,g}+(1-\alpha)L_{s,\text{SUB}}-\alpha(1-\alpha)L_{g,\text{SUB}}. \quad (3)\end{aligned}$$

In a similar way, R_{eff} can be obtained from the law of power conservation [6]. If the Eddy current loss is neglected, the total power consumption of the system can be represented as

$$\begin{aligned}\tfrac{1}{2}R_{\text{eff}}I^2 &= R_gI_0^2+\tfrac{1}{2}R_sI^2+\tfrac{1}{2}R_{\text{SUB}}I_2^2\\ &=\tfrac{1}{2}\alpha^2\tfrac{1}{2}R_gI^2+\tfrac{1}{2}R_sI^2+\tfrac{1}{2}(1-\alpha)^2R_{\text{SUB}}I^2 \quad (4)\end{aligned}$$

or

$$R_{\text{eff}}=\alpha^2\tfrac{1}{2}R_g+R_s+(1-\alpha)^2R_{\text{SUB}}. \quad (5)$$

R_{eff} can be expressed in a similar form as (3)

$$\begin{aligned}R_{\text{eff}} &= \alpha\left(\tfrac{1}{2}R_g+R_s\right)+(1-\alpha)(R_{\text{SUB}}+R_s)\\ &\quad-\alpha(1-\alpha)\left(\tfrac{1}{2}R_g+R_{\text{SUB}}\right). \quad (6)\end{aligned}$$

From (3) and (6), it is interesting to note that the system can be regarded as the combination of a coplanar line system without a substrate, a quasi-microstrip line system with a substrate serving as the return path (between a signal line and silicon substrate), and a line system between ground lines with the substrate return path. C_{eff} and G_{eff} can be expressed by the components in Fig. 2(b) as

$$C_{\text{eff}}=\frac{G_t^2C_{\text{ox}}+\omega^2C_{\text{ox}}C_{\text{SUB}}(C_{\text{ox}}+C_{\text{SUB}})}{G_t^2+\omega^2(C_{\text{ox}}+C_{\text{SUB}})^2}+C_{sm} \quad (7)$$

$$G_{\text{eff}}=\frac{\omega^2C_{\text{ox}}^2G_t}{G_t^2+\omega^2(C_{\text{ox}}+C_{\text{SUB}})^2} \quad (8)$$

where the admittances $G_{\text{eff}}+j\omega C_{\text{eff}}$ is given as

$$G_{\text{eff}}+j\omega C_{\text{eff}}=\frac{1}{\dfrac{1}{1/(G_t+j\omega C_{\text{SUB}})+1/j\omega C_{\text{ox}}}+\dfrac{1}{j\omega C_{sm}}}.$$

In the expression for L_{eff} and R_{eff} in (3) and (6), α as defined in (1) is given as an unknown parameter. However, a general expression for α is difficult to obtain because of its dependence on factors such as structure, frequency, and electromagnetic interaction between lines. An approximate value for α can be obtained if we assume that the system can be separated by two isolated parallel line systems: a coplanar line system without substrate and a quasi-microstrip line system with the substrate serving as the return path (one between the signal line and silicon substrate).

TABLE IV
GEMETRICAL AND ELECTRICAL DATA FOR CASES "A," "B," AND "C" IN FIGS. 4 AND 5 [2]. THE METAL THICKNESS IS ASSUMED TO BE 0.7 μm FOR THE CALCULATIONS OF L_{eff} AND C_{eff} (AS REFERRED TO IN [3])

Items	"A"	"B"	"C"
W_s (μm)	4.8	9.6	2.0
W_g (μm)	20	20	20
R_s (kΩ/m)	15.5	7.4	20
R_g (kΩ/m)	3.5	3.6	2
S_m (μm)	100	100	100
T_{ox} (μm)	0.57	0.58	0.5
substrate conductivity (S/m)	800	15.5	100

In the above approximation, the voltage drops V_g and V_{SUB} on a coplanar line and a quasi-microstrip line per unit length, respectively, can be considered to be the same, and can be expressed as

$$V_g\approx Z_gI_1=\left(\frac{1}{2}R_g+j\omega L_{s,g}\right)I_1 \quad (9)$$

$$V_{\text{SUB}}\approx Z_{\text{SUB}}I_2=(R_{\text{SUB}}+j\omega L_{s,\text{SUB}})I_2. \quad (10)$$

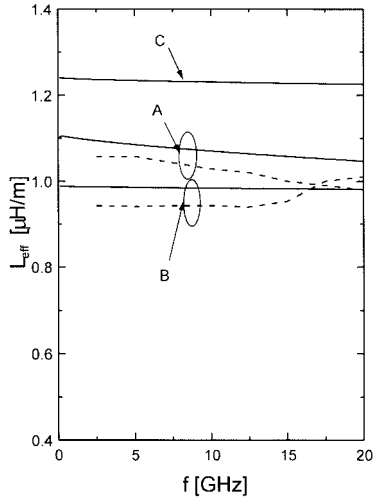
Equating V_g and V_{SUB}, α can be written as

$$\alpha=\frac{|Z_{\text{SUB}}|}{|Z_g|+|Z_{\text{SUB}}|} \quad (11)$$

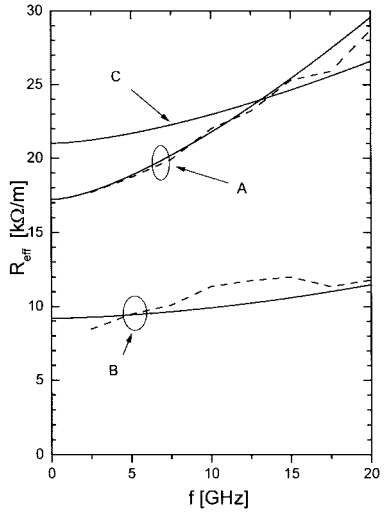
where $|Zg|=\sqrt{(R_g/2)^2+(\omega L_{s,g})^2}$ and $|Z_{\text{SUB}}|=\sqrt{R_{\text{SUB}}^2+(\omega L_{s,SUB})^2}$.

From (3) and (6), L_{eff} and R_{eff} have been expressed as a combination of three components multiplied by three current ratio terms α, $1-\alpha$, and $\alpha(1-\alpha)$. If the effect of the $\alpha(1-\alpha)$ term on impedance is small compared with the other two terms, the system becomes, approximately, a combination of two isolated systems (a coplanar system and microstrip system). Our method for obtaining α can be regarded as a perturbation method since the system is assumed to be composed of two isolated systems.

Before a comparison study using test results, the proposed model is compared using the reported experimental data for silicon substrates having three different doping concentrations, as tabulated in Table IV [2]. Fig. 4(a) and (b) shows the frequency dependence of L_{eff} and R_{eff}, respectively. Fig. 4(a) shows that both the proposed model (solid line) and reported experimental data (dotted line) predict that L_{eff} decreases slightly with increasing frequency for all cases. This trend can be explained by the fact that the current flow through a substrate seeks a minimal impedance path, respective to L_{eff} as the inductive resistance increases at high frequency. In addition, R_{eff} increases with increasing frequency, as shown in Fig. 4(b). In Fig. 4(b), the rate of increase in R_{eff} is strongly dependent on substrate doping concentrations, indicating the importance of the substrate as a return path. As expected from (7) and (8), C_{eff} and G_{eff} are clearly dependent on frequency, as shown in Fig. 5(a) and (b). This is especially so for the case of low doping (see Table IV, case "B"). Both the proposed

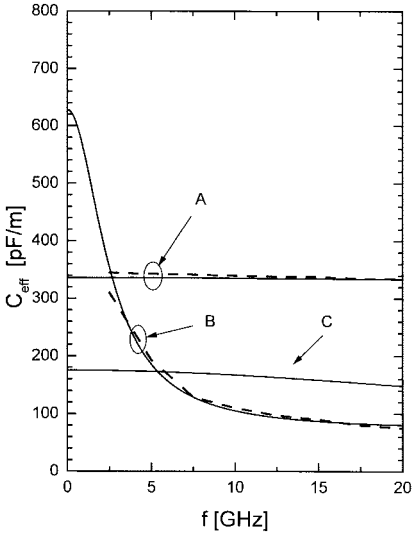


(a)

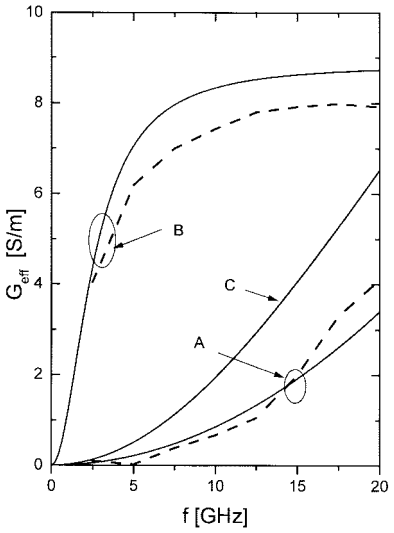


(b)

Fig. 4. (a) $L_{\rm eff}$ and (b) $R_{\rm eff}$ versus frequency for cases "A," "B," and "C," as tabulated in Table IV. Dotted lines are taken from the reported measurements [2] and solid lines are derived from the proposed model.



(a)



(b)

Fig. 5. (a) $C_{\rm eff}$ and (b) $G_{\rm eff}$ versus frequency for cases "A," "B," and "C," as tabulated in Table IV. Dotted lines are taken from the reported measurements [2] and solid lines are derived from the proposed model.

model (solid line) and the reported experiment (dotted line) in $C_{\rm eff}$ show an extremely strong dependence on frequency. All $G_{\rm eff}$ fits well and is within 15% of the reported experimental values, although the error is larger for the substrate with low conductivity (see Table IV, case "B").

III. Experiments

For the characterization of the interconnects on the silicon substrate, a test pattern, shown in Fig. 1, was designed and measured. The test pattern contains splits in the width of the signal lines, and the ground lines alternate for shielding the electromagnetic flux leakage. The signal lines are spit into widths of 1, 2, 4, 10, and 20 μm, and the ground line widths are fixed at 100 μm. The space between the signal and ground line is large enough (over 90 μm) to accommodate the wafer probes. This space also guarantees negligible microloading effects during the metal-etching process, which can deform the signal line deformation from an ideal rectangular shape. The top and bottom pads ($D1$ and $D1'$) are used for deembedding the parasitic capacitances of the signal line pads. All lines are 5000 μm in length. The interconnects are composed of 6600-Å-thick aluminum on the barrier metal, which is 300 Å in thickness. The multistacked oxides layered on the interconnects is approximately 4 μm in thickness. The silicon substrate under the oxide layer whose thickness is 0.87 μm is composed of p-well (with an average conductivity of near 45 S/m and depth of 2.5 μm) on the p-substrate wafer (having a conductivity of near 15 S/m and a depth of 660 μm). The high-frequency measurements on this structure have been performed using an network analyzer and coplanar microwave probes for contacting the devices using test methods similar to those adopted by Eo and Eisenstadt [7].

The complex characteristic impedance and complex propagation constant were derived from the measured S-parameters after subtracting the capacitive effects of the contact pads. Fig. 6(a) shows the real and imaginary parts of the characteristic impedance as functions of frequency, along with

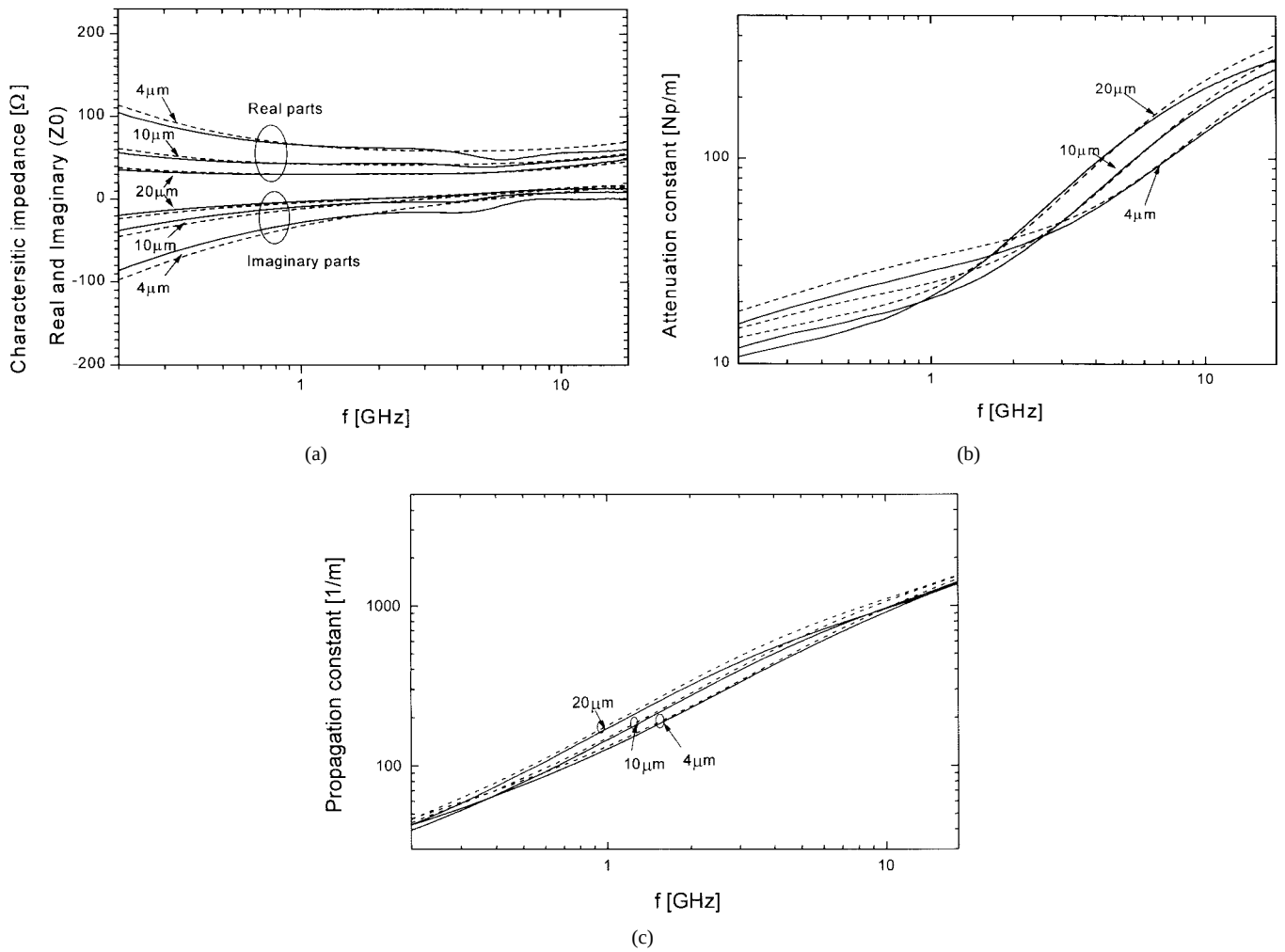


Fig. 6. Results from measurements and proposed (a) complex characteristic impedance, (b) attenuation, and (c) propagation constant versus frequency for signal lines having three different signal widths. Dashed line: proposed model. Solid line: measurement.

the attenuation constant of each line in Fig. 6(b). At high frequencies, losses in the substrate become important in the attenuation, and the effect increases as line width increases, whereas the substrate effect is negligible at low frequencies since the ohmic resistance of metal lines dominates the losses [3]. As expected, Fig. 6(c) shows that the dependence of propagation constant on line widths decreases as the frequency increases [3]. As seen in these figures, the agreement between models and measurements is quite good and the model predicts the general trend in the frequency characteristics of the coplanar line with the substrate.

The effective resistance and capacitance of the lines (Fig. 3) are analyzed in Figs. 7 and 8 because a silicon substrate effect strongly appears on these parameters. Data from the numerical simulation using Raphael[1] are also shown in these figures. In the Raphael simulation, the effect of the substrate on line parameters are not included. In the relatively low-frequency region, Fig. 7(a) shows that the difference between the measured (solid line) and simulated results (dashed line: model, dotted line: Raphael) is larger for smaller metal line widths, which is the result of the microloading effect. As frequency increases, $R_{\rm eff}$'s, based on measurements and our proposed model, increase faster than the data from the Raphael simulation without the substrate effect. Subsequently, we found that the difference is caused by the substrate effect on the total line resistance. Fig. 7(b) shows $W_s R_{\rm eff}$ versus frequency, which should be constant with respect to variation in the frequency and W_s variation if $R_{\rm eff}$ is dependent only on metal line resistances. However, $W_s R_{\rm eff}$ is a strong function of frequency and its dependency varies with W_s. From (5), $W_s R_{\rm eff}$ can be written as

$$W_s R_{\rm eff} = W_s(R_s + \alpha^2 \tfrac{1}{2} R_g) + W_s(1-\alpha)^2 R_{\rm SUB}. \quad (12)$$

The rapid increase in $W_s R_{\rm eff}$ at the high frequency for larger W_s cannot be explained without considering the substrate as the return path, although the resistance increase due to the metal skin effect is included in Raphael simulation, as shown in Fig. 7(a). The last term of the right-hand side (RHS) is approximately linearly dependent on W_s (if dependence of α and $R_{\rm SUB}$ on W_s is negligible), whereas the first term is insensitive (note that $R_s \propto 1/W_s$ and $R_g \ll R_s$ in our test patterns). It is responsible for a large increase in $R_{\rm eff}$ since $R_{\rm SUB}$ is several hundreds or thousands of times larger than R_s. It is clear that, even though the amount of the current flow through the substrate is negligible, its effect on $R_{\rm eff}$ is not.

Fig. 8 shows $C_{\rm eff}$ versus frequency for signal lines of different widths, and that the frequency dependence increases

[1]TMA Raphael Manual, San Francisco, CA 1994.

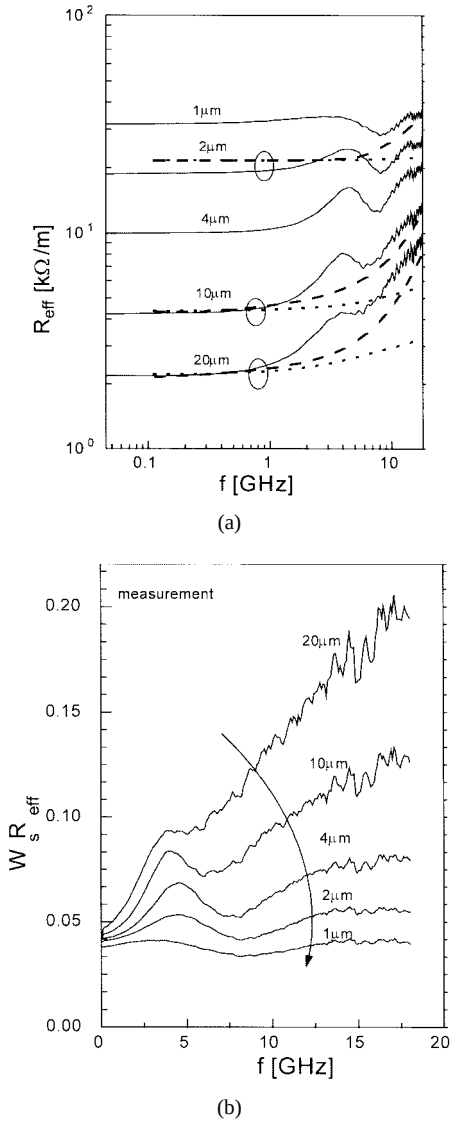


Fig. 7. (a) R_{eff} as a function of various signal line widths versus frequency and (b) $W_s R_{\text{eff}}$ according to signal line widths versus frequency. Solid line: measurement. Dashed line: proposed model. Dotted line: Raphael (reference).

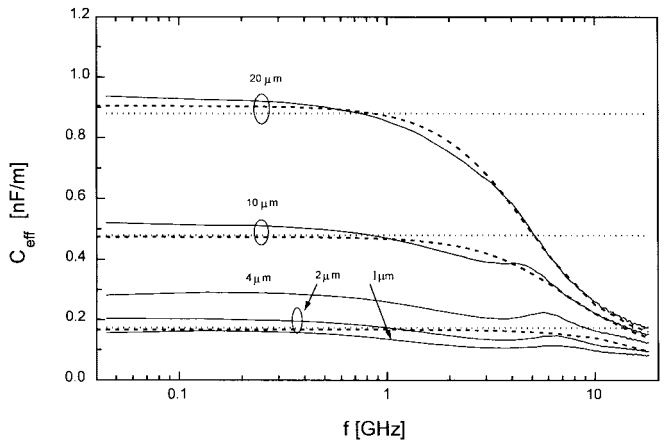


Fig. 8. C_{eff} as a function of various signal line widths versus frequency. Solid line: measurement. Dashed line: proposed model. Dotted line: Raphael (reference).

as W_s increases. A C_{eff} approaches $C_{\text{ox}} + C_{sm}$, C_{eff} for the low frequency limit and becomes the quasi-TEM limit capacitance C_d at a high-frequency limit as

$$C_d = \frac{C_{\text{ox}} C_{\text{SUB}}}{C_{\text{ox}} + C_{\text{SUB}}} + C_{sm}. \tag{13}$$

The good agreement of the numerical simulation without considering the substrate effect with the measurements (and the proposed model) at low frequency shows that the silicon substrate can be considered a conductor metal for frequencies lower than 1 GHz, for the conductor system considered in this paper. This suggests that the substrate can be considered as a metal plain in the C_{eff} modeling up to several gigahertz, and C_{eff} is nearly the same as C_{ox} ($C_{\text{eff}} \cong C_{\text{ox}}$) since C_{sm} is small. The slight difference between the measured and simulated data at low frequency in Fig. 8 results from the process variation in the dielectric constant of the insulators and line-width deformations [8]. The proposed model shows excellent agreement with the measured capacitances for a wide range of frequency. In the proposed model and Raphael simulations, the complicated dielectric materials have been taken into account for the calculation of the capacitances [7].

The model described in this paper is based on energy and power conservation, and includes the silicon substrate as a current return path. The effective cross-sectional area A_{SUB}, which is important in determining various parameters, is assumed to have a simple form, as is shown in (A3). W_{SUB} is set to be W_s for the signal line of large width [4] and is set to be S_m for that of small width. Empirically, the above values give reasonable R_{SUB}, but more elaboration is needed to obtain better value. In calculating R_{SUB} [see Appendix, (A4)] [4], [9], we included a correction factor F, defined by $\mu_0/(4L_{s,g})$. F includes the information on the nonuniform magnetic flux in the space between signal and ground lines. Since the magnetic flux induces the return current in a silicon substrate, the effective resistance is influenced by the constant F, which can be considered a geometric factor. The reasonable agreement with the measurement, which has been demonstrated in the previous section, justifies the model for A_{SUB} and R_{SUB}, but additional consideration is required for other geometrics. F changes slightly if the system geometry is changed. Finally, the validity of the proposed model in the calculation of the current ratio α in (11) should be carefully reviewed. Fig. 9 shows the frequency dependence of the current ratio from (11). Below 20 GHz, the ratio is greater than 0.9 for the three cases in Table IV, and the small value of $\alpha(1-\alpha)$ in (3) is thus guaranteed. It is possible to predict the dependence of the distributed electrical parameters on the geometry and frequency since our model contains an analytic formula. In (12), it is possible to ascertain the importance of the substrate path and its dependence on the width of signal interconnect, as well as frequency. Fig. 10 shows the effective substrate resistance $(1-\alpha)^2 R_{\text{SUB}}$ as a function of frequency from the proposed model, as well as the numerical simulation [2]. The effective substrate resistance from the proposed model is slightly dependent on line widths, as mentioned earlier, whereas that from the numerical simulation is not. In addition, it should be noted from Figs. 7, 8, and 10 that if the width of the signal interconnect lines is scaled down below 1 μm for given frequency ranges (MHz $\sim$ 10 GHz), the effect of the

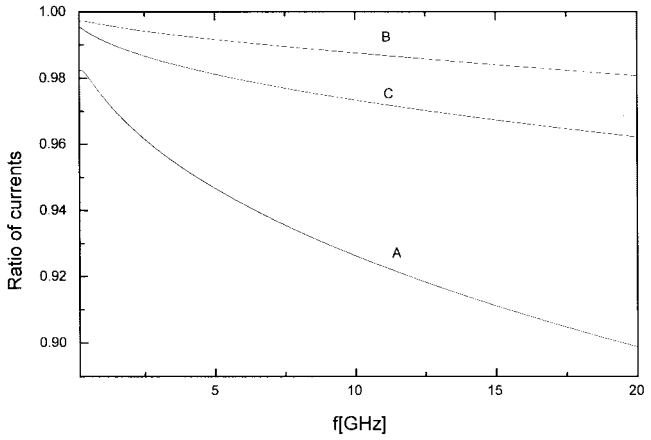


Fig. 9. Current distribution ratio α versus frequency for cases "A," "B," and "C" in Table IV.

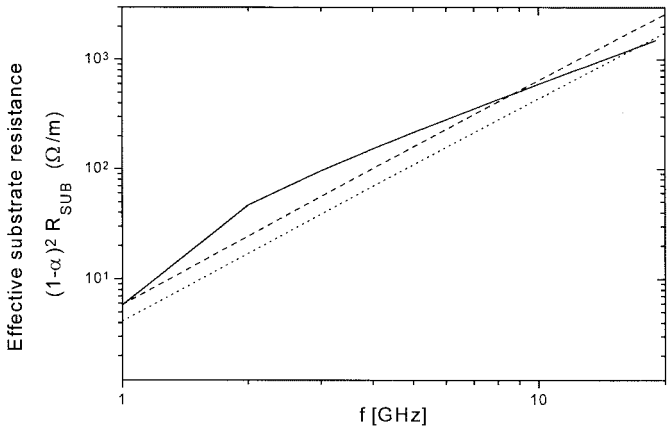


Fig. 10. Effect of current flow through the silicon substrate on $R_{\rm eff}$ as a function of frequency. Dashed and dotted line: proposed model $W_s = 0.5\ \mu$m and $W_s = 20\ \mu$m, respectively. Solid line: numerical simulations [2].

substrate on the resistance is negligible, and the difference between the dc-based model and proposed model in the VLSI on-chip interconnection performance is negligible.

IV. Conclusion

A simple formula is proposed for the analysis of electrical parameters of the interconnect system, including the substrate effect. From a comparison between measurements and the proposed model, it is clear that models developed in this study can be used for the accurate estimation of the distributed electrical parameters ($R_{\rm eff}$, $L_{\rm eff}$, $C_{\rm eff}$, and $G_{\rm eff}$) of the interconnects system, including the substrate effect.

Appendix

For the formula of elements in Table II, the self inductance L and mutual inductance M [10] are first given as

$$L = Al\left[\ln\left(\frac{4l}{p}\right) + \frac{1}{2}\right] H \tag{A1}$$

$$M = Al\left[\ln\left(\frac{l}{d} + \sqrt{1+\left(\frac{l}{d}\right)^2}\right) - \sqrt{1+\left(\frac{d}{l}\right)^2} + \frac{d}{l}\right] H \tag{A2}$$

TABLE V
Distances and Perimeters Used in the Appendix for the Inductances Calculation

Items	Perimeter (p) or Distance (d)
perimeter of a signal line	$p_s=2(W_s+T_s)$
perimeter of a ground line	$p_g=2(W_g+T_g)$
perimeter of a substrate as a current path	$p_{SUB}=2(S_m+T_{sp})$
distance between signal-to-ground line	$d_s=S_m+(W_g+W_s)/2$
distance between ground-to-ground line	$d_g=2S_m+W_g+W_s$
distance between signal-to-substrate	$d_{SUB}=T_{ox}+T_{sp}/2$
distance between ground-to-substrate	$d_{g\text{-}SUB}=(d_g^2+d_{SUB}^2)^{1/2}$

where l and p are the length and perimeter of a conductor (meter–kilogram–second (MKS) unit), respectively, d is the geometric mean distance between two conductors (MKS unit), and A is a constant of 2×10^{-7}. If the length of conductors is sufficiently long, each inductance is calculated using (A1), (A2), and the elements tabulated in Table V, i.e., $L_s = L(l, p_s)$, $L_{\rm SUB} = L(l, p_{\rm SUB})$, and $L_g = L(l, p_g)$ for self inductances and $M_{s-g} = M(l, d_s)$, $M_{s-{\rm SUB}} = M(l, d_{\rm SUB})$, $M_{g-g} = M(l, d_g)$, and $M_{g-{\rm SUB}} = M(l, d_{g-{\rm SUB}})$ for mutual inductances.

Secondly, the cross-sectional area $A_{\rm SUB}$ of the current path in the silicon substrate is given as

$$A_{\rm SUB} = W_{\rm SUB} T_{sp} \tag{A3}$$

where $W_{\rm SUB}$ is given as $W_{\rm SUB} = W_s$ for $W_s > S_m/2$ and $W_{\rm SUB} = S_m$ (see Table I) otherwise, respectively.

The longitudinal resistance $R_{\rm SUB}$ [4], [9] can be rewritten as (per unit length)

$$R_{\rm SUB} = \frac{3}{\sigma_{sp} F A_{\rm SUB}}. \tag{A4}$$

where F is defined as $\mu_0/(4L_{s,g})$, and μ_0 is the permeability of vacuum.

The standard metal equation for the metal resistance R_m used in this paper is given as

$$R_m (= R_{ac}) = \frac{1}{\sigma_m \delta_m \left[1 - \exp\left(-\frac{T_m}{\delta_m}\right)\right](T_m + W_m)}, \quad \text{if } R_{dc} < R_{ac}$$

$$(= R_{dc}) = \frac{1}{\sigma_m T_m W_m}, \qquad \text{otherwise} \tag{A5}$$

where σ_m and δ_m are defined as the metal conductivity and metal skin depth, respectively [7].

Based on the "quasi-TEM" model [4], the capacitances C_{sm}, $C_{\rm SUB}$, and conductance G_t, shown in the Table III, can be written as

$$C_{sm} = \frac{1}{2c^2 L_{s,g}} \tag{A6}$$

$$C_{\rm SUB} = \epsilon_{si} C_{sm} \tag{A7}$$

$$G_t = C_{sm} \frac{\sigma_{sp}}{\epsilon_{si}} \tag{A8}$$

where c, ϵ_{si}, and σ_{sp} are defined as the velocity of light in vacuum, relative dielectric constant of a silicon substrate, and silicon conductivity, respectively. Also, the capacitance $C_{\rm ox}$ is written as

$$C_{\rm ox} = W_s \frac{\epsilon_0 \epsilon_{\rm ox}}{T_{\rm ox}} + C_f \text{ (per unit length).} \tag{A9}$$

The following empirical equation is used for the fringing capacitance C_f of the signal interconnect [11]:

$$C_f = \epsilon_0 \epsilon_{er\,\rm eff} \cdot \left(\frac{2\pi}{\ln\left[1 + 2\frac{T_{\rm ox}}{T_s} + \sqrt{2\frac{T_{\rm ox}}{T_s}\left(\frac{2T_{\rm ox}}{T_s} + 2\right)}\right]} - \frac{T_s}{2T_{\rm ox}} \right) \tag{A10}$$

where the relative dielectric constant $\epsilon_{er\,\rm eff}$ is determined by the stacked dielectric materials [7].

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Hun-Sup Park, photograph and biography not available at the time of publication.